WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a capacitor configured by a bottom electrode, a top electrode, and a dielectric disposed between the bottom electrode and the top electrode;

an insulating layer which surrounds the capacitor; and

a high-dielectric which is disposed between the dielectric and the insulating layer, and which entirely covers side wall portions of the dielectric,

wherein a dielectric constant of the high-dielectric is higher than a dielectric constant of the insulating layer.

2. The semiconductor device according to claim 1, wherein the dielectric constant of the high-dielectric is higher than a dielectric constant of the dielectric configuring the capacitor.

3. The semiconductor device according to claim 1, wherein a thickness of the high-dielectric in a direction perpendicular to side surfaces of the dielectric configuring the capacitor is equal to a distance from the bottom electrode to the top electrode.

4. The semiconductor device according to claim 1, wherein the insulating layer is silicon oxide.

5. The semiconductor device according to claim 1, wherein the high-dielectric is configured by any one of

SiN, TaO_2, TiO_2, Al_2O_3, ZrO_2, HfO_2, BST, PZT, and SBT.

6. The semiconductor device according to claim 1, wherein the high-dielectric covers the bottom electrode and the top electrode.

7. The semiconductor device according to claim 1, wherein the high-dielectric covers only side wall portions of the dielectric.

8. The semiconductor device according to claim 1, wherein, between the high-dielectric and the dielectric configuring the capacitor, a barrier layer to prevent reaction of the high-dielectric and the dielectric is disposed.

9. A semiconductor device comprising:

a first capacitor and a second capacitor each of which is configured by a bottom electrode, a top electrode, and a dielectric disposed between the bottom electrode and the top electrode;

an insulating layer which surrounds the first capacitor and the second capacitor; and

a high-dielectric which are disposed between the dielectric and the insulating layer, and which entirely covers side wall portions of the dielectric,

wherein a dielectric constant of the high-dielectric is higher than a dielectric constant of the insulating layer.

10. The semiconductor device according to claim 9, wherein the insulating layer and the high-dielectric

exist at a space between the first capacitor and the second capacitor.

11. The semiconductor device according to claim 9, wherein only the high-dielectric exists at a space between the first capacitor and the second capacitor.

12. A semiconductor device comprising:

a capacitor configured by a bottom electrode, a top electrode, and a dielectric disposed between the bottom electrode and the top electrode;

a transistor which is connected to the bottom electrode;

an insulating layer which surrounds the capacitor; and

a high-dielectric which is disposed between the dielectric and the insulating layer, and which entirely covers side wall portions of the dielectric,

wherein a dielectric constant of the high-dielectric is higher than a dielectric constant of the insulating layer.

13. A manufacturing method for a semiconductor device, comprising:

forming a first conductive material;

forming a dielectric on the first conductive material;

forming a second conductive material on the dielectric;

forming a top electrode formed from the second

conductive material by etching on the second conductive material and the dielectric;

forming a high-dielectric which entirely covers side surfaces of the dielectric, and which has a dielectric constant higher than that of an insulating layer;

forming a bottom electrode formed from the first conductive material by etching on the high-dielectric and the first conductive material; and

forming the insulating layer which covers the bottom electrode, the top electrode, and the high-dielectric.

14. The manufacturing method according to claim 13, wherein the high-dielectric and the first conductive material are etched by using a hard mask as a mask.

15. The manufacturing method according to claim 13, wherein, after the high-dielectric is etched, the first conductive material is etched by using a hard mask formed from the high-dielectric as a mask.

16. The manufacturing method according to claim 15, wherein an etching selectivity is controlled such that the high-dielectric does not exist at the top portion of the top electrode at a point in time when the etching on the first conductive material is completed.

17. The manufacturing method according to

claim 13, wherein the high-dielectric is etched by etch back, and remains at only the side wall portions of the dielectric.

18. The manufacturing method according to claim 17, wherein, after the high-dielectric is etched, the first conductive material is etched by using a hard mask as a mask.